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NOTICE OF ALLOWANCE AND FEE(S) DUE

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08/15/2008

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005

EXAM	IINER
JAIN,	RAJ K
ART UNIT	PAPER NUMBER

2616

DATE MAILED: 08/15/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,498	10/29/2003	Abbas Amirichimeh	1875.3640003/JTH/TAD	8175

TITLE OF INVENTION: CROSS LINK MULTIPLEXER BUS CONFIGURED TO REDUCE CROSS-TALK

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1440	\$300	\$0	\$1740	11/17/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

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PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.			JAIN,	RAJ K
1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005		ART UNIT	PAPER NUMBER	
			2616	

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1022 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1022 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Ar	plication No.	Applicant(s)
10	/695,498	AMIRICHIMEH ET AL.
Matica of Allowability	aminer	Art Unit
RA	J K. JAIN	2616
The MAILING DATE of this communication appears All claims being allowable, PROSECUTION ON THE MERITS IS (OR herewith (or previously mailed), a Notice of Allowance (PTOL-85) or o NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGH of the Office or upon petition by the applicant. See 37 CFR 1.313 and	on the cover sheet wing REMAINS) CLOSED in their appropriate commuts. This application is s	th the correspondence address n this application. If not included unication will be mailed in due course. THIS
1. This communication is responsive to <u>7/3/08</u> .		
2. X The allowed claim(s) is/are 4-7,11-14 and 18 renumbered 1-9.		
 3. Acknowledgment is made of a claim for foreign priority under a) All b) Some* c) None of the: 1. Certified copies of the priority documents have been copies of the priority documents have been copies of the certified copies of the priority documents have been copies of the certified copies of the priority documents 	en received. en received in Applicatio	on No
International Bureau (PCT Rule 17.2(a)).		
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" of the noted below. Failure to timely comply will result in ABANDONMEN' THIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 4. A SUBSTITUTE OATH OR DECLARATION must be submitted INFORMAL PATENT APPLICATION (PTO-152) which gives re-	Γ of this application. . Note the attached EXA	AMINER'S AMENDMENT or NOTICE OF
5. CORRECTED DRAWINGS (as "replacement sheets") must be		
(a) ☐ including changes required by the Notice of Draftsperson's		w (PTO-948) attached
1) hereto or 2) to Paper No./Mail Date .	T dient Branning Previer	. (110010) attached
(b) ☐ including changes required by the attached Examiner's An Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1.84(o	:)) should be written on th	he drawings in the front (not the back) of
each sheet. Replacement sheet(s) should be labeled as such in the h 6. DEPOSIT OF and/or INFORMATION about the deposit of attached Examiner's comment regarding REQUIREMENT FOR	of BIOLOGICAL MATE	ERIAL must be submitted. Note the
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5 ☐ Notice of In	formal Patent Application
·	6. Interview S	ummary (PTO-413),
2. Notice of Draftperson's Patent Drawing Review (PTO-948)		(Mail Data
 Notice of Draftperson's Patent Drawing Review (PTO-948) Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>5/8/07</u> 	Paper No./ 7. ⊠ Examiner's	Amendment/Comment

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Timothy Doyle on March 14, 2008.

- Claims 1-3, 8-10 and 15-17 have been canceled.
- Claim 18 has been added.
- Claims 4 and 11 have been amended as follows;
- 4. (Currently Amended) A cross link multiplexer bus, comprising:
- a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal and an origin port configured to produce said signal; and
- a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein:

said signal is eapable of being configured to be represented as a series of characters, and a character of said series of characters is eapable of being configured to be represented as a first data bit, a second data bit, and a first control bit;

a first interconnect of said set of interconnects is configured to convey said first data bit, a second interconnect of said set of interconnects is configured to convey said second data bit, and a third interconnect of said set of interconnects is configured to convey said first control bit;

Page 3

said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk;

said third interconnect is positioned substantially between said first interconnect and said second interconnect;

said series of characters is further configured to be represented as a third data bit, a fourth data bit, and a second control bit;

a fourth interconnect of said set of interconnects is configured to convey said third data bit, a fifth interconnect of said set of interconnects is configured to convey said fourth data bit, and a sixth interconnect of said set of interconnects is configured to convey said second control bit; and

said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

11. (Currently Amended) A cross link multiplexer bus, comprising:

a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive a signal, an origin port configured to produce said signal, a first power supply configured to provide a first voltage, and a second power supply configured to provide a second voltage, said first voltage <u>is</u> different from said second voltage; and

a plurality of interconnects, wherein a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers of said plurality of cross link multiplexers;

wherein:

said signal is eapable of being configured to be represented as a series of characters, and a character of said series of characters is eapable of being configured to be represented as a first data bit and a second data bit;

a first interconnect of said set of interconnects is configured to convey said first data bit, a second interconnect of said set of interconnects is configured to convey said second data bit, and a third interconnect of said set of interconnects is configured to convey one of said first voltage and said second voltage;

said first interconnect, said second interconnect, and said third interconnect are configured in a manner to reduce cross-talk;

said third interconnect is positioned substantially between said first interconnect and said second interconnect;

said <u>character of series</u> of characters is further configured to be represented as a third <u>data</u> bit and a fourth data bit;

a fourth interconnect of said set of interconnects is configured to convey said third data bit, a fifth interconnect of said set of interconnects is configured to convey said fourth data bit, and a sixth interconnect of said set of interconnects is configured to convey one of said first voltage and said second voltage; and

Application/Control Number: 10/695,498 Page 5

Art Unit: 2616

said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

18. (New) A cross link multiplexer bus, comprising:
a first cross link multiplexer;
a second cross link multiplexer;
a destination port coupled to one of the first cross link multiplexer and the second cross
link multiplexer and configured to receive a signal, wherein the signal is configured to be
represented as a series of characters, a character of said series of characters is configured to be
represented as a first data bit, a second data bit, a first control bit, a third data bit, a fourth data
bit, and a second control bit;
an origin port coupled to one of the first cross link multiplexer and the second cross link
multiplexer and configured to produce the signal;
a first interconnect coupled between the first cross link multiplexer and the second cross
link multiplexer and configured to convey the first data bit;
a second interconnect coupled between the first cross link multiplexer and the second
cross link multiplexer and configured to convey the second data bit;
a third interconnect coupled between the first cross link multiplexer and the second cross
link multiplexer, said third interconnect positioned between the first interconnect and the second
interconnect in a manner to reduce cross talk, and configured to convey one of the first control
bit, a power supply voltage, and a ground voltage;

a fourth interconnect coupled between the first cross link multiplexer and the second cross link multiplexer and configured to convey the third data bit;

a fifth interconnect coupled between the first cross link multiplexer and the second cross link multiplexer and configured to convey the fourth data bit; and

a sixth interconnect coupled between the first cross link multiplexer and the second cross link multiplexer, said sixth interconnect positioned between the fourth interconnect and the fifth interconnect in a manner to reduce cross talk, and configured to convey one of the second control bit, the power supply voltage, and the ground voltage.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

Claim 4 is allowed;

The prior art discloses plurality of cross link multiplexers interconnected via set of interconnects from a plurality of interconnects and configured to receive and transmit data between the multiplexers and other devices as appropriate.

The prior art however fails to disclose a signal configured to be represented as a series of characters, and a character of said series of characters is configured to be represented as a first data bit, a second data bit, a first control bit, a third data bit, a fourth data bit, and a second control bit, and furthermore the cross link multiplexers having a fourth interconnect of said set of interconnects configured to convey said third data bit, a fifth interconnect of said set of interconnects configured to convey said fourth data bit, and a sixth interconnect of said set of interconnects configured to convey a

second control bit and said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

Claim 11 is allowed;

The prior art discloses plurality of cross link multiplexers interconnected via set of interconnects from a plurality of interconnects and configured to receive and transmit data between the multiplexers and other devices as appropriate.

The prior art however fails to disclose a signal configured to be represented as a series of characters and a character of said series of characters is configured to be represented as a first data bit, a second data bit, a third data bit, and a fourth data bit, and further the cross link multiplexers having a fourth interconnect of said set of interconnects configured to convey said third data_bit, a fifth interconnect of said set of interconnects configured to convey said fourth data_bit, and a sixth interconnect of said set of interconnects is configured to convey one of a first voltage and a second voltage wherein the first voltage is different from the second voltage and said sixth interconnect is positioned substantially between said fourth interconnect and said fifth interconnect.

Claim 18 is allowed;

The prior art discloses plurality of cross link multiplexers interconnected via set of interconnects from a plurality of interconnects and configured to receive and transmit data between the multiplexers and other devices as appropriate.

The prior art however fails to disclose a signal configured to be represented as a series of characters and a character of said series of characters is configured to be represented as a first data bit, a second data bit, first control bit, a third

data bit, a fourth data bit, and a second control bit, and further the cross link multiplexers having a fourth interconnect of said set of interconnects configured to convey said third data_bit, a fifth interconnect of said set of interconnects configured to convey said fourth data_bit, and a sixth interconnect positioned between the fourth interconnect and the fifth interconnect in a manner to reduce cross talk, and configured to convey one of the second control bit, a power supply voltage, and a ground voltage.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAJ K. JAIN whose telephone number is (571)272-3145. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

Application/Control Number: 10/695,498 Page 9

Art Unit: 2616

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Raj K. Jain/

Art Unit 2616
August 14, 2008

/Chi H Pham/ Supervisory Patent Examiner, Art Unit 2616 8/11/08